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EdXact and Altos Partner to Improve IP Characterization Throughput

Combined flow offers 2X- 4X reduction in library characterization runtime

San Jose, California and Grenoble, France – July 15, 2009 – Altos Design Automation Inc. and EdXact SA today announced that they are partnering to further improve characterization turn-around time especially for large cells and macro blocks.

Through the Altos Pal O'Altos partnership program, the two companies have developed an integrated flow between Altos ultra-fast characterization products (Liberate™, Variety™ and Liberate™ MX) and EdXact's Jivaro™ parasitic reduction platform. The combined solution delivers a 2X improvement in library characterization performance when used on a commercial 40nm standard cell library with nearly identical results. For larger intellectual property (IP) blocks such as complex I/O cells and memory instances, the run-time improvement is even more significant, often 4X or more. The integrated flow between the two partners includes smart exploitation of advanced features of the Jivaro engine such that the required accuracy is always maintained.

Mathias Silvant, president and CEO of EdXact said, "Our company knowledge on parasitics analysis and reduction is recognized worldwide. We have had experiences with different design types, like large memory blocks, RF blocks, analog and mixed-signal applications. Altos' productivity improvement confirms the good results we had with major semiconductor companies on library characterization. Becoming a partner with Altos will further help the smooth integration of our tools and the performance of our partners' flows.

Jim McCanny, Altos CEO and founder said, "The number of library corners required to enable advanced System-on-Chip (SoC) design has increased dramatically as has the complexity of the underlying IP components due to the need to manage power and the impact of process variation. Consequently .IP characterization is a significant bottleneck in any chip design process especially as re-characterization is often required to ensure accurate correlation between the IP and the ever-shifting silicon process. By partnering with EdXact we are able to offer yet another significant boost to IP characterization turn around time without any significant accuracy tradeoff. This enables design teams to get the most accurate up to date models they require in hours rather than weeks or months."

Availability and demonstration

Jivaro is available from EdXact, the interface to Jivaro is available in Liberate, Variety and Liberate MX from Altos. For more information, contact Jim McCanny at jmccanny@altos-da.com or 408-980-8056 x103 or Mathias Silvant at silvant@edxact.com or +33476668980.

The combined flow will be demonstrated at this year's Design Automation Conference (San Francisco July 26-30) at Altos' booth (booth number 1504). The Jivaro tools will be demonstrated at EdXact's booth (booth number 3765).

About EdXact

Founded in 2004, EdXact SA focuses on electronic design tools aimed at physical verification tasks. EdXact's innovative model order reduction technology helps accelerate extensive backend verifications in complex IC design cycles. EdXact is headquartered in Grenoble area, France, with sales offices in Japan, Korea, Israel, Taiwan and India. <http://www.edxact.com>

About Altos

Altos Design Automation provides ultra-fast, fully-automated characterization technology for the creation of library views for timing, signal integrity and power analysis and optimization. Altos advanced modeling solutions are used by both corner-based and statistical-based design implementation flows to reduce time to market and improve yield.

Privately held, Altos was founded in 2005 in Santa Clara, CA. Its corporate headquarters is at 4020 Moorpark Ave., Suite 100, San Jose, CA 95117. Telephone: (408) 980-8056. On the Web at: <http://www.altos-da.com>

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